THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOBIA SAADEH

Appeal No. 95-5064
Application 08/049,463[1]

ON BRIEF

Before MARTIN, BARRETT, and FLEMING, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision in an appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-3 and 5-8 under § 103 as unpatentable for obviousness over prior art. Claim 4 stands

[1] Application for patent filed April 20, 1993.

objected for depending from a rejected claim. Independent claim 9 and its dependent claims 10-12 have been allowed. We reverse.

The claimed invention relates to hold-up circuitry for supplying power to a load (e.g., a computer) during momentary interruptions of the voltage source. The hold-up circuit includes power storage means (e.g., a capacitor) for providing voltage to the load during voltage source interruptions and safety means for preventing the continuation of discharge from the power storage means when the voltage being provided to the load drops below the predetermined level at which the load is designed to operate.

Claim 1 is illustrative of the invention and reads as follows:

1. In combination with a source of power, an electrical load connected to the source for operation at an operating voltage above a predetermined level, hold-up circuit means for maintaining said operation of the load during momentary interruption in power of the source, comprising: power storage means connected to the load for supply of said operating voltage thereto, impedance means connected to the power storage means for regulating charge thereof and discharge thereof into the load during said interruption in power of the source and safety means responsive to a drop in voltage applied to the load from the source below said predetermined level for preventing continuation of said discharge of the power storage means into the load during said interruption in power of the source.

The sole reference relied on by the examiner is:

Konopka	4,709,320	Nov. 24, 1987

All of the appealed claims (i.e., claims 1-3 and 5-8) stand rejected under 35 U.S.C. § 103 as unpatentable for obviousness over Konopka. Although Appellant's brief states (at 4) that the claims do not stand or fall together, the only claim that is specifically argued in the brief is claim 1. Accordingly, we will treat claims 2, 3, and 5-8 as standing or falling with claim 1. In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986).

Konopka discloses a circuit for shutting down a PWM (pulse width modulation) power supply 16 (Fig. 1) when a low voltage detector 20 determines that the input DC voltage ("HIGH DC") at power supply input terminal 15 drops below a predetermined level for a predetermined period of time (e.g., 13 ms). Under these circumstances, the low voltage detector 20 outputs a signal via a latch circuit 22 to a shut down circuit 24, which issues a PWM OFF signal and a DATA SAVE signal. Referring to Figure 2, which shows the details of the low voltage detector 20, the collector of transistor 40 is at ground potential when the input DC voltage at terminal 15 is at or above an acceptable level. When the input voltage drops below that level, the collector voltage increases, causing capacitor 38 to charge through resistor 36. If the input voltage remains low for

a long enough period of time (e.g., 13 ms), the voltage on the capacitor reaches the threshold voltage (e.g., 20 volts) of a voltage-sensitive switching device 42, which then quickly discharges the capacitor through LED 46 in a photo-optic coupler 44. The light pulse emitted by the LED drives the phototransitor 48 in the photo-optic coupler into conduction for about 50 µs, thereby generating a 5-volt pulse for application to the latch circuit, which triggers the shut down circuit.

The examiner contends, and Appellant does not dispute, that it would have been obvious to connect peripheral computer equipment to the output terminals 18 ("LOW DC") of Konopka's power supply 16, thereby satisfying the requirement of claim 1 for "an electrical load connected to the source for operation at an operating voltage above a predetermined level." As a result, the sole question before us is whether Konopka thus modified satisfies the remaining limitations of the claim. For the following reasons, we agree with Appellant that the answer is no, because Konopka thus modified does not include the claimed "power storage means connected to the load for supply of said operating voltage thereto" or the claimed "impedance means connected to the power storage means for regulating . . . discharge thereof into the load during said interruption in power of the source."

Whether read on capacitor 38 alone or in combination with one or more of switching circuit 42, photo-optic coupler 44, latch circuit 22, and shut down circuit 24, Konopka's power storage means does not discharge through the load connected to power supply output terminals 18, as required to satisfy the claim. Instead, the only current that reaches the load is the current generated by the power supply itself. The only effect of capacitor 38, switching circuit 42, photo-optic coupler 44, latch circuit 22, and shut down circuit 24 on the power supply is to turn it off when the input voltage thereto on line 15 remains too low for too long. As a result, we cannot sustain the rejection of claim 1 or of claims 2, 3, and 5-8, which stand or fall (in this case stand) therewith.

REVERSED

JOHN C. MARTIN Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES

)
MICHAEL R. FLEMING)
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